IP Timer2 Module

Mike Shea and Mike Kucera
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This note describes a four channel predet timer, implemented as an IndustryPack™† module, using an Actel-1240 field programmable gate array. The 1240 gate array is a user programmable chip that can be configured and programmed locally in the Actel development system. The Timer Module receives the 10 MHz Tevatron event clock, decodes events, outputs up to eight detected events and four programmable delay pulses. These delayed pulses are referenced to a selectable clock events or to an externally generated trigger.

Physically, the IndustryPack Module is a 1.8" by 3.9" circuit board that contains two high density 50-pin "D" female connectors as defined by the GreenSpring IndustryPack specification. This specification is a public domain definition of a small mezzanine board for use in microprocessor-based systems. Figure 1 is a diagram of the IP Timer 2 module showing the parts placement including the two 50-pin connectors, one logic interface and one for user I/O signals. The logic interface includes:

D0-D15	16 bit data
IOSEL/	I/O Addr space select
INTSEL/	Interrupt Select
INTREQ0	Interrupt request
ACK/	Acknowledge
R-W/	Read-Write control
Addr 1..6	I/O space Address lines
Reset/	Clears all registers, inhibits triggers (low active)

At the present time, the Actel chip does not assert an interrupt request, but interrupt capability could be added into the Actel design if required. The Actel chip contains the following circuitry:

- IP logic interface
- 2 Control/Status register
- Tevatron-style event clock decoder
- Trigger event register
- Three 16-bit delay counter
- Four 16-bit delay comparators
- Divide by 10 clock prescaler

The Actel chip outputs all detected 8-bit events along with their *data valid* strobe to a 22V10 PAL. The 22V10 can be separately programmed to output selected events or combinations of events to the octal 25-ohm buffer. Two 74F3037 4-bit 50-ohm buffers drive the four delayed strobes, the reference strobe that triggered the timers, the 10 MHz clock recovered from the input event clock, and two copies of the input clock. A 10 MHz oscillator included on the board can be selected for use as a local timebase.

The input Tevatron clock is received by a discriminator that has a self tracking reference input. This design eliminates the need to adjust the input discriminator level for various amplitude input signals. A second discriminator clamps the output of the first discriminator in the absence of an input signal.

Registers in the Actel part are mapped into the Industry-Pack I/O space. An *IOSEL* is generated at a selected base address by the carrier board to allow word access to the gate array registers. Figure 2 shows Actel pinout and the register map of the module. The chip is initialized by loading the delay values into the first four words, the triggering event into the least significant byte of word addresses $xx08 and $xx0C, and the control register contents into the least significant byte of addresses $xx0A and $xx0E. Bits in the control register can be set to individually enable the functions shown in Figure 3. These include:

- Enabling the delay timer outputs
- Prescaling the 10 MHz timebase
- Selecting: External 10 MHz timebase
  Event trigger
  Offboard trigger
  Onboard trigger from the 22V10
  Output pulse length
  Enable daisychain mode

Figure 4 gives the pinout of the 50-pin carrier board connector.

Inside the Actel part, the delay comparators for channels 0 and 1 compare against a single 16-bit counter. As the counter increments, a match is found a delayed output pulse is generated. Comparators 2 and 3 compare the stored delay value against two separate counters. When the daisychain mode is selected, channel 2 and 3 counters may be started by the delayed output pulses of channels 0 and 1, respectively. This design allows one or two *START and WIDTH* pulse pairs to be generated to control devices that cannot tolerate receiving an *OFF* pulse before receiving an *ON* pulse. Also, changing the *START* time of such a pair will not change the value of the *WIDTH*. Daisychaining 0 to 2 is controlled by Control Register bit 0 (CR00). Daisychaining 1 to 3 is controlled by bit CR10. All other CR0 bits 7..1 affect timers 0 and 1, and

CR1 bits 7..1 affect timers 2 and 3. Functions of the control register bits are given in Figure 3.

Although the IP module described here has been designed as a predet timer , the board itself can serve as a platform for testing or building other Actel designs. The basic board provides an Actel chip with an IndustryPack connection to a carrier board, three dedicated external inputs, and two bytes of buffered digital I/O. Data direction of signals to the octal I/O buffer is controlled by an Actel chip output. The 22V10 can be used or bypassed. Using this board, it should be possible to easily implement special devices such as pulse counters, pulse burst generators, and high speed stepping motors.

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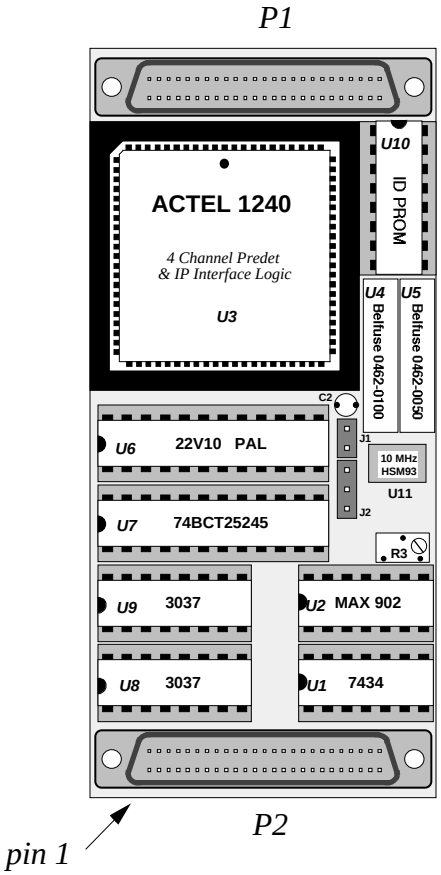


Industry Pack–Based 4-Channel Predet Module
IPTimer2

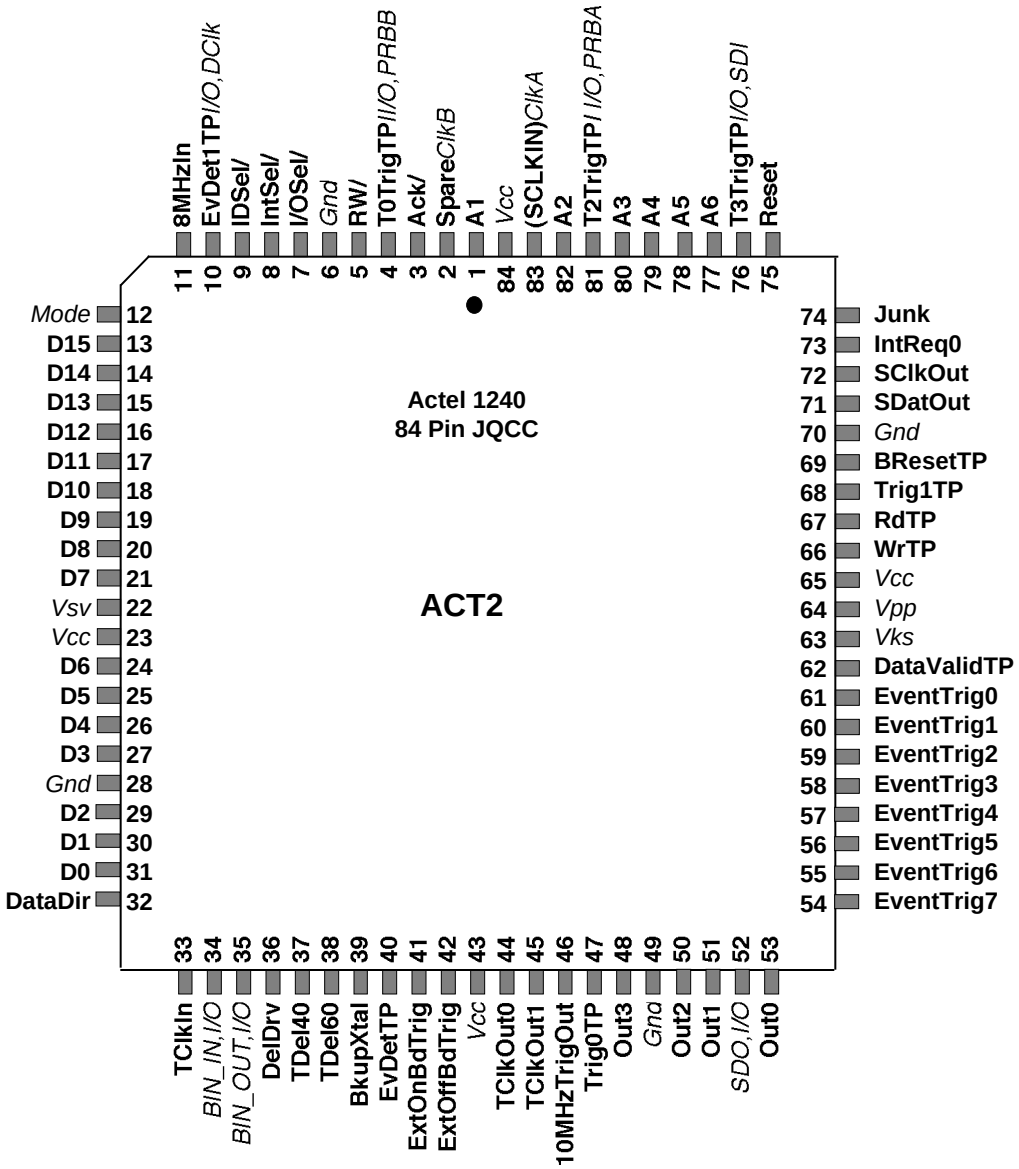


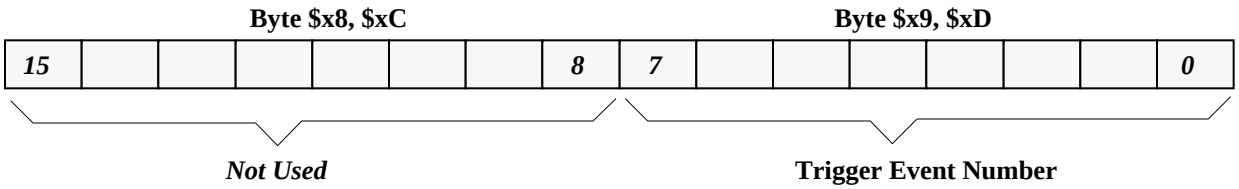
Figure 2a. IP Timer 2 Actel Pinout

Address	R/W	Function
Base + 0	R/W	Channel 0 delay
Base + 2	R/W	Channel 1 delay
Base + 4	R/W	Channel 2 delay
Base + 6	R/W	Channel 3 delay
Base + 8	R/W	Trigger Event 0
Base +A	R/W	Control Register 0
Base + C	R/W	Trigger Event 1
Base + E	R/W	Control Register 1

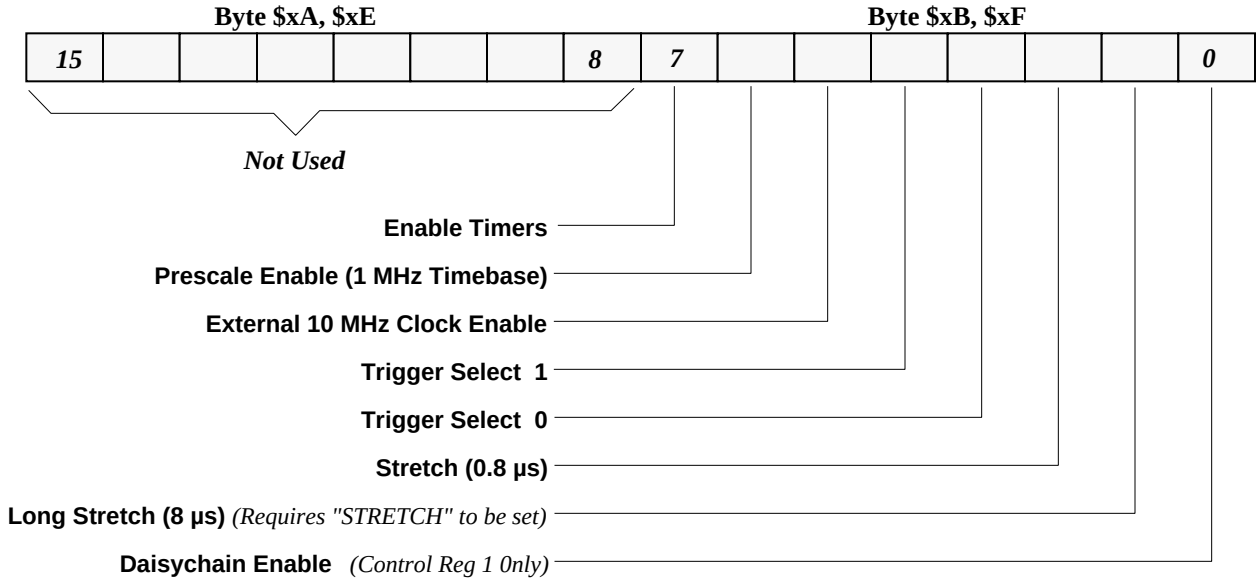
Note: Only Word Accesses are Supported
Trigger Event and Control Registers occupy the low byte

Figure 2b. IP Timer 2 Address Map

Event Register



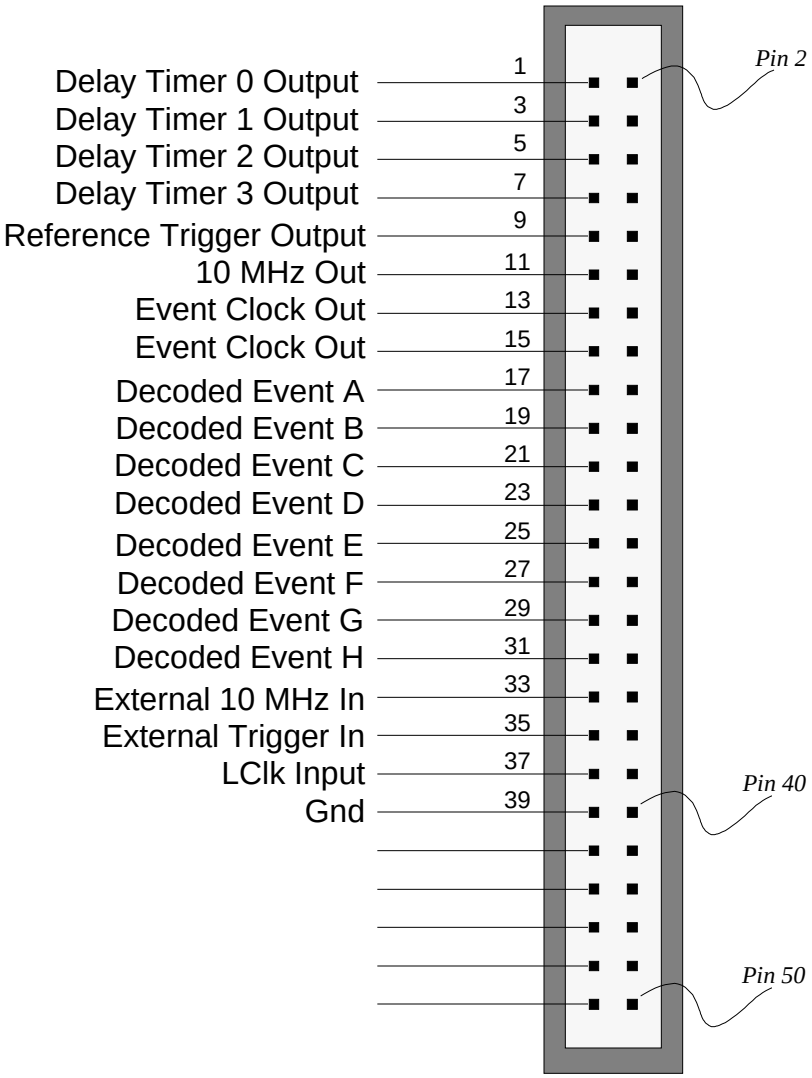
Control Register



Trigger Select	Trigger Source
0 1 2 3	15Hz Reset Event Detect Onboard External Trigger Offboard Extrenal Trigger

Figure 3. Control Registers for IP Timer2 Gate Array

m/s 011593



Notes: All Even Numbered Pins are Gnd.
Pin numbers of the IP module connector P2 are the same as for Carrier Board connector

Figure 4. IP Carrier Board I/O Connector Pinout for Timer 2 Connector